Opportunities and Challenges of III-V Nanoelectronics for Future High-Speed, Low-Power Logic Applications

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Abstract*—This paper highlights the opportunities and challenges of III-V nanoelectronics for future high-speed, low-power digital logic applications. III-V materials in general have significantly higher electron mobility than Si and can potentially play a major role along with Si in future high-speed, low-power computing. The major potential advantage of using a III-V quantum-well field-effect transistor as a logic transistor is that it can be operated under very low supply voltage (e.g., 0.5 V), and hence, lower power dissipation while still achieving very high speed. Compared to other emerging high-mobility materials, such as, carbon nanotubes and semiconductor nanowires, which require "bottom-up" chemical synthesis for formation and suffer from the fundamental placement problem, III-V materials are far more practical in terms of patterning. However, many significant challenges remain to be overcome before III-V materials become applicable for future high-speed, low-power logic applications. These include (i) finding a compatible high-κ gate dielectric on III-Vs, (ii) demonstrating gate length scalability below 35 nm with acceptable I_{ON}/I_{OFF} ratio, (iii) improving the hole mobility in III-Vs or finding the right p-channel FET for the complementary metal-oxide-semiconductor (CMOS) configuration, and (iv) integrating III-V materials onto the Si substrate.

Keywords*—Nanoelectronics, III-V materials, quantum-well, field-effect transistors, digital logic.

I. Introduction

Recently there has been much interest generated and good progress made in the study of non-Si electronic materials, such as carbon nanotubes (CNTs), semiconductor nanowires and III-V materials, for future high-speed and low-power computation applications [1, 2]. These materials, in general, have significantly higher intrinsic mobility (either higher electron or hole mobility) than Si, and they can potentially be used to replace Si as the channel of the transistor for very high speed applications. Both CNTs and semiconductor nanowires are formed using "bottom-up" chemical synthesis, and they currently suffer from the fundamental placement problem, i.e., there is no practical and reliable way to precisely align and position them. On the other hand, III-V materials can be patterned into desirable device structures using conventional "top-down" lithographic and etch techniques. In this regard, III-Vs are considered far more practical than CNTs and nanowires for future high-speed device applications. In fact, III-V materials have been used in communication and optoelectronic products for quite some time.

III-V materials have ~50-100× higher electron mobility than Si, and the resulting III-V quantum-well field-effect transistors (QWFETs) are showing some very attractive and tangible merits over scaled Si MOSFETs [3, 4]. However, there still remain many difficult challenges to overcome before these III-V devices can replace scaled Si MOSFETs for future high-speed, low-power CMOS logic applications. But if we can solve these problems, III-V materials can play a major role in future high-speed and low-power computational devices, along with Si. The objective of this paper is to highlight the opportunities and challenges of III-V nanoelectronics, especially the III-V quantum-well FETs, for potential future high-speed and low-power logic applications.

II. Opportunities

III-V materials, in general, have much higher electron mobility than Si [5]. Figures 1 and 2 show the electron mobility and conductivity, respectively, as a function of the charge carrier density measured in various III-V quantum well structures [6-40]. The III-V quantum well layer is sandwiched between the wider-bandgap III-V barrier layers. The III-V barrier layers are needed for (i) carrier confinement in the quantum well and (ii) for junction leakage and transistor off-state leakage current I_{OFF} reduction. The wider bandgap barrier layers may also be counterdoped, that is, p-type barriers for n-channel QWFETs, to further mitigate short channel effects. The data shows that with the exception of GaN, most III-V quantum wells exhibit higher electron mobility and conductivity than Si. InSb shows the highest electron mobility and conductivity but it also has the lowest bandgap of 0.18 eV. Pseudomorphic $In_xGa_{1-x}As$ quantum

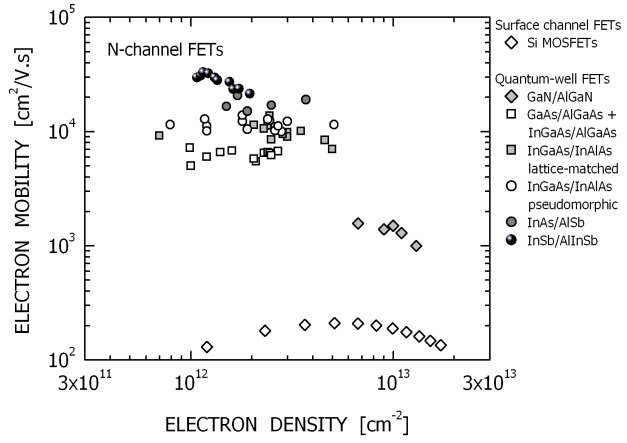

Fig. 1. Electron mobility μ versus sheet electron density n_S in n-channel FETs: Si MOSFETs [6], GaN/AlGaN QWFETs [7-12], GaAs/AlGaAs and InGaAs/AlGaAs QWFETs [13-20], lattice-matched InGaAs/InAlAs QWFETs [21-27], pseudomorphic InGaAs/InAlAs QWFETs [28-35], InAs/AlSb QWFETs [36-40], and InSb/AlInSb QWFETs [3].

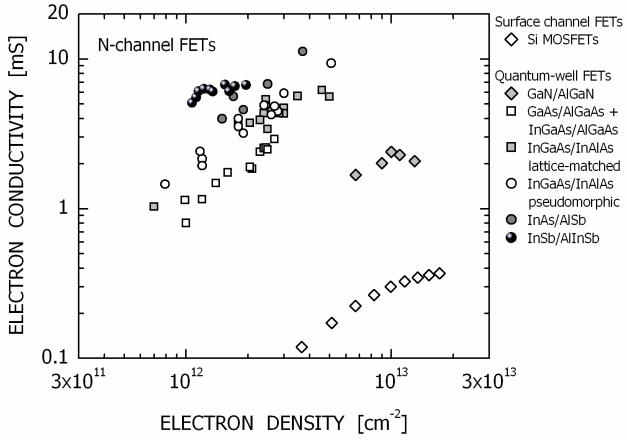

Fig. 2. Electron conductivity $q\mu n_S$ versus sheet electron density n_S in n-channel FETs: Si MOSFETs [6], GaN/AlGaN QWFETs [7-12], GaAs/AlGaAs and InGaAs/AlGaAs QWFETs [13-20], lattice-matched InGaAs/InAlAs QWFETs [21-27], pseudomorphic InGaAs/InAlAs QWFETs [28-35], InAs/AlSb QWFETs [36-40], and InSb/AlInSb QWFETs [3].

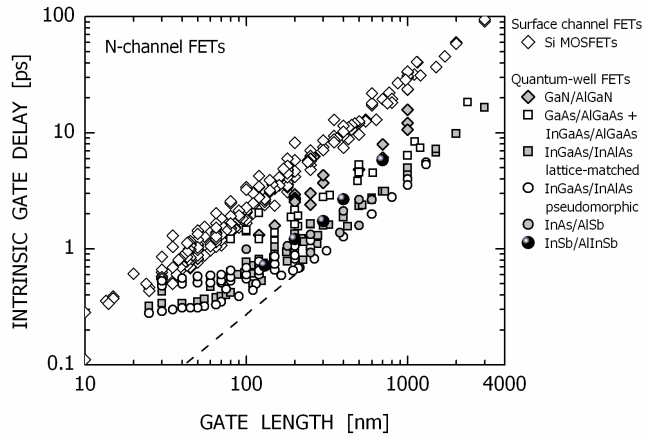

Fig. 3. Intrinsic gate delay *CV/I* versus physical gate length L_G of n-channel FETs: Si MOSFETs [6], GaN/AlGaN QWFETs [7-12], GaAs/AlGaAs and InGaAs/AlGaAs QWFETs [13-20], lattice-matched InGaAs/InAlAs QWFETs [21-27], pseudomorphic InGaAs/InAlAs QWFETs [28-35], InAs/AlSb QWFETs [36-40], and InSb/AlInSb QWFETs [3]. The dashed line indicates the projected *CV/I* in the absence of source and drain parasitic resistances (see Fig. 5 for details).

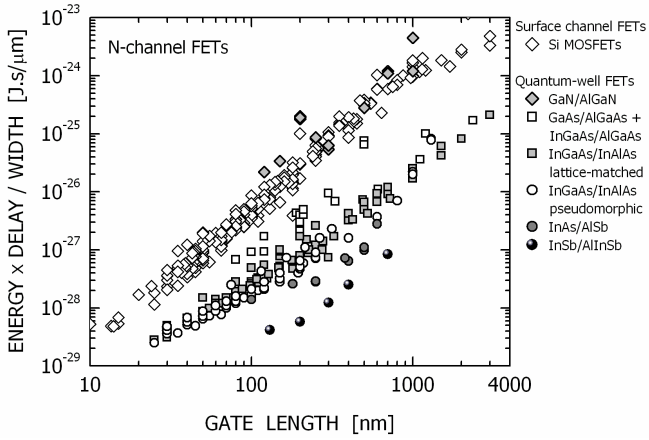

Fig. 4. Energy-delay product versus physical gate length L_G of n-channel FETs: Si MOSFETs [6], GaN/AlGaN QWFETs [7-12], GaAs/AlGaAs and InGaAs/AlGaAs QWFETs [13-20], lattice-matched InGaAs/InAlAs QWFETs [21-27], pseudomorphic InGaAs/InAlAs QWFETs [28-35], InAs/AlSb QWFETs [36-40], and InSb/AlInSb QWFETs [3].

wells with $x > 0.53$ are also very attractive in terms of electron mobility and conductivity. In addition, these materials have a higher bandgap ranging from 0.55 to 0.74 eV depending on the In mole fraction. Band-to-band tunneling in these narrow bandgap high-mobility quantum wells can be mitigated by lowering the drain field in the quantum well by optimizing the barrier thickness [5].

High electron mobility and conductivity give rise to high transistor drive current at both low drain (I_{DLIN}) and high drain bias (I_{DSAT}), which are very important for high speed logic applications. The linear drive current I_{DLIN} is directly proportional to the conductivity. The saturated drive current I_{DSAT} in short-channel FETs is proportional to the carrier density, as well as the carrier injection velocity above the source-to-channel potential barrier which in turn depends on the low-field carrier mobility and effective mass *m** [41-43]. Fundamentally, III-Vs have lower carrier density than Si due to lower density of states, as shown in Figures 1 and 2. However, due to the lower *m** and higher mobility in III-Vs, the injection velocity is high enough to more than compensate the lower carrier density. This is evident in Figures 3 and 4, which show that III-V quantum-well FETs have higher intrinsic speed, i.e., lower gate delay *CV/I*, and lower energy-delay product than Si MOSFETs at a given transistor gate length L_G. In these figures, gate delay for the III-V quantum-well FETs is determined from the measured values of unity-gain cutoff frequency f_T using $CV/I = 1/2\pi f_T$ while gate capacitance is estimated using $C_{gs} = \varepsilon_b/(L_b + \Delta L)$, where ε_b and L_b are the dielectric constant and the thickness of the barrier layer, respectively, and ΔL is the separation of the peak electron density from the barrier/well interface.

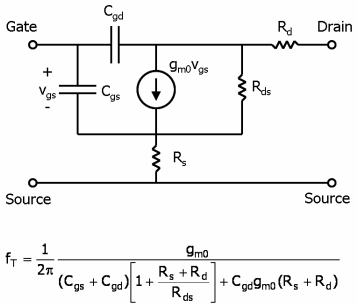

Fig. 5. Small-signal equivalent circuit model of a FET and an expression for unity-gain cutoff frequency f_T. C_{gs} and C_{gd} are the gate-to-source and the gate-to-drain capacitances, v_{gs} is the small-signal gate-to-source voltage drop across C_{gs}, g_{m0} is the intrinsic transconductance, R_s and R_d are the source and drain parasitic resistances, and R_{ds} is the FET output resistance.

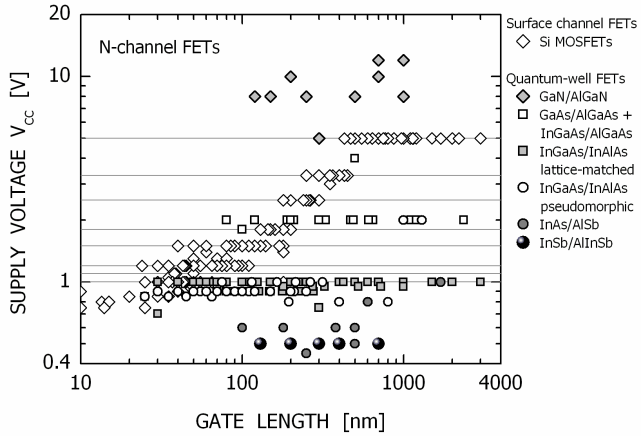

Fig. 6. Supply voltage V_{CC} versus gate length L_G of n-channel FETs: Si MOSFETs [6], GaN/AlGaN QWFETs [7-12], GaAs/AlGaAs and InGaAs/AlGaAs QWFETs [13-20], lattice-matched InGaAs/InAlAs QWFETs [21-27], pseudomorphic InGaAs/InAlAs QWFETs [28-35], InAs/AlSb QWFETs [36-40], and InSb/AlInSb QWFETs [3]. The horizontal lines indicate the V_{CC} values used by the Si industry: 5, 3.3, 2.5, 1.8, 1.5, 1.2, 1.1, and 1.0 V.

Most of the III-V quantum-well FETs considered here show significant improvement in gate delay CV/I and energy-delay product over Si MOSFETs. However it is also observed that the gain tends to "saturate" with reducing transistor gate length L_G. This saturation can be explained using the small-signal equivalent circuit model of a FET, as shown in Figure 5, which shows the importance of parasitic source and drain resistances R_s and R_d, and output resistance R_{ds} on unity-gain cutoff frequency f_T. Reducing the gate-to-source and gate-to-drain distances using a self-aligned technology should reduce R_s and R_d while reducing the gate-to-channel separation should improve short-channel effects, hence increasing R_{ds}. It is then expected that the performance improvement trend will continue with L_G scaling as shown by the dashed line in Figure 3.

The main motivation of researching III-V devices for logic applications is really the possibility of achieving high device speed at low supply voltage V_{CC} (e.g., ~ 0.5 V). III-V quantum well transistors, having significantly higher electron mobility than Si, may provide such a path, as shown in Figure 6.

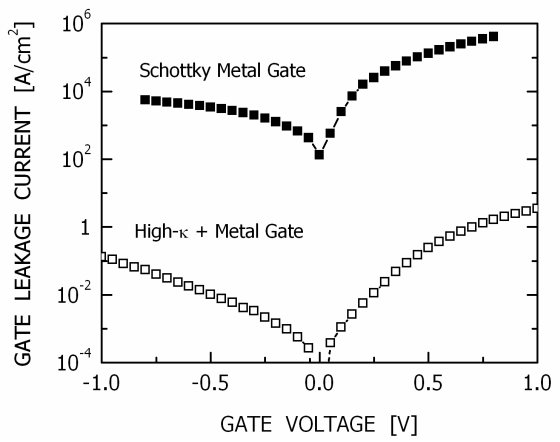

Fig. 7. Gate leakage current versus gate voltage for III-V Schottky metal gate stack and III-V/high-κ/metal-gate stack [47].

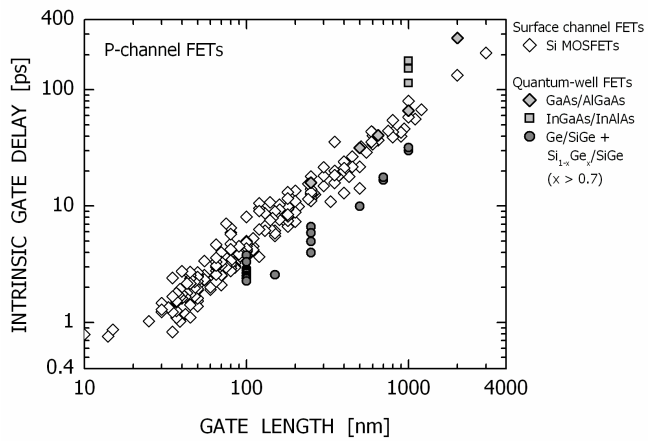

Fig. 8. Intrinsic gate delay CV/I versus gate length L_G of p-channel FETs: Si MOSFETs [5], GaAs/AlGaAs QWFETs [48], lattice-matched and pseudomorphic InGaAs/InAlAs QWFETs [49], and strained Ge/SiGe and strained $Si_{1-x}Ge_x$/SiGe (x > 0.7) QWFETs [50-60].

III. CHALLENGES

III-V quantum-well transistors still have many difficult challenges that need to be overcome before they can be considered useful for logic applications. Currently, all of these devices use a Schottky metal gate and do not have a gate dielectric stack. This results in a large vertical Schottky gate leakage, which in turn causes high transistor off-state leakage I_{OFF} [3]. A gate dielectric stack which is compatible with III-Vs [44-46] will need to be incorporated in the III-V quantum-well device to (i) reduce I_{OFF} and (ii) improve gate control and subthreshold slope, and therefore, enhance device scalability. Figure 7 shows the reduction of the vertical gate leakage with the use of a high-κ/metal-gate stack on III-V. At present, such a gate stack on III-V is showing fast surface states and CV instability, which needs to be eliminated [47].

For III-V devices to be competitive versus scaled Si MOSFETs, their physical gate lengths L_G need to be scaled to 35 nm and below with acceptable I_{ON}/I_{OFF} ratio, for example, $I_{ON}/I_{OFF} > 1000$ at $V_{CC} = 0.5$ V. Moreover, for direct coupled

FET logic (DCFL) applications, one needs both depletion-mode (normally ON) and enhancement-mode (normally OFF) transistors. Recently significant breakthroughs have been made in this regard: both depletion- and enhancement-mode III-V quantum-well n-channel FETs with 85 nm L_G have been demonstrated with high performance at a V_{CC} of only 0.5 V. These results will be presented at the IEDM 2005 [4].

For CMOS logic applications, there is a need for p-channel FETs with very high hole mobility. Currently III-V materials are showing hole mobility comparable to Si, which results in gate delay CV/I that is comparable to that of Si as shown in Figure 8 [48, 49]. The challenge here involves either improving the hole mobility in III-Vs, such as, compressively strained III-V quantum well approach or finding the correct p-channel FET using other novel materials, such as, Ge quantum wells, as shown in Figure 8 [50-60].

Finally, III-V materials will need to be integrated selectively onto the Si platform. Significant challenges remain for monolithic integration of III-Vs on Si, such as, (i) the anti-phase boundary defects, (ii) thermal mismatch issues, and (iii) lattice mismatch problem [61-65]. III-V materials will not replace Si; rather, they will need to be integrated onto Si as the channel material for future high-speed, low-power logic transistors.

IV. Summary

While III-V quantum-well FETs show some very attractive and tangible merits, there exist many difficult challenges to overcome before they will become applicable for future high-speed, low-power logic applications. If the problems are indeed solved, III-Vs can play a major role along with Si in future logic nanoelectronics. Finally, III-Vs will not replace Si and they will need to be integrated onto the Si substrate.

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